# RG20A_EVKIT Mnual

Circuit boards for evaluation RG20 analog 8ch input and output



DD0-0900010A0

**Active Low**

(1) Setting number of slots per cycle

RG20 series allow 4,8, 16, 32, 64 and 128 slots per cycle.
Following is the table of number of slots per cycle setting.

| Slots | nS7 | nS6 | nS5 | nS4 | nS3 | nS2 | nS1 | nS0 |
|---|---|---|---|---|---|---|---|---|
| 4 | L | L | L | L | L | H | * | * |
| 6 | L | L | L | L | H | * | * | * |
| 16 | L | L | L | H | * | * | * | * |
| 32 | L | L | H | * | * | * | * | * |
| 64 | L | H | * | * | * | * | * | * |
| 128 | H | * | * | * | * | * | * | * |

(2) Setting SS ( Sending Slot)

Pins in lower (right hand) order than the first pin from the left
with value "H" are used to specify SS (Sending Slot) Number.
For example, if the number of slots per cycle is "4",
the first pin from the left with value "H" is nS2.
So nS1 and nS0 are used to specify SS from 0 to 3.

| SS | nS7 | nS6 | nS5 | nS4 | nS3 | nS2 | nS1 | nS0 |
|---|---|---|---|---|---|---|---|---|
| 0 | L | L | L | L | L | H | H | H |
| 1 | L | L | L | L | L | H | H | L |
| 2 | L | L | L | L | L | H | L | H |
| 3 | L | L | L | L | L | H | L | L |

(3) Setting RS ( Receiving Slot)

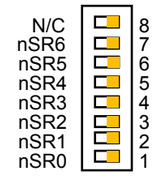
RS is always the value of SS with inverted MSB.

| SS | RS |
|---|---|
| 0 | 2 |
| 1 | 3 |
| 2 | 0 |
| 3 | 1 |

S1


Setting Number of Slots and SS/RS

S3



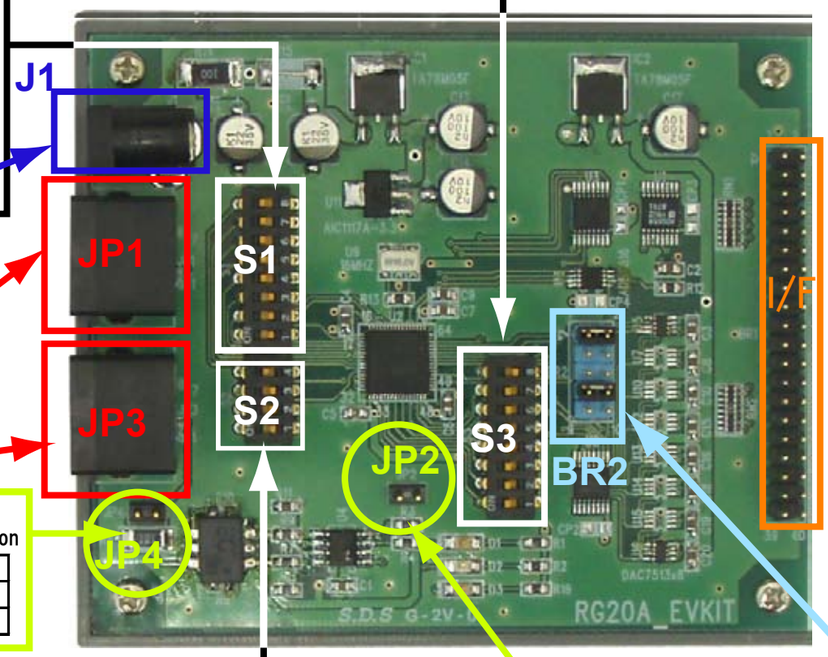

Slew-rate Setting

nSR0 - nSR6

In a characteristic to appoint a bit to admit a change,
when the bit set nSR "L", it's necessary for setting lower bit nSR "L".

| change bit | nSR6 | nSR5 | nSR4 | nSR3 | nSR2 | nSR1 | nSR0 |
|---|---|---|---|---|---|---|---|
| ADIN[3:0] | H | H | H | H | H | H | H |
| ADIN[4:0] | H | H | H | H | H | H | L |
| ADIN[5:0] | H | H | H | H | H | L | L |
| ADIN[6:0] | H | H | H | H | L | L | L |
| ADIN[7:0] | H | H | H | L | L | L | L |
| ADIN[8:0] | H | H | L | L | L | L | L |
| ADIN[9:0] | H | L | L | L | L | L | L |
| ADIN[10:0] | L | L | L | L | L | L | L |

**Active Low**




General I/F MIL40

| Use | PIN | PIN | Use |
|---|---|---|---|
| 12V | 1 | 2 | 12V |
| 12V | 3 | 4 | 12V |
| ADIN8 | 5 | 6 | GND |
| ADIN7 | 7 | 8 | GND |
| ADIN6 | 9 | 10 | GND |
| ADIN5 | 11 | 12 | GND |
| ADIN4 | 13 | 14 | GND |
| ADIN3 | 15 | 16 | GND |
| ADIN2 | 17 | 18 | GND |
| ADIN1 | 19 | 20 | GND |
| DAOUT8 | 21 | 22 | GND |
| DAOUT7 | 23 | 24 | GND |
| DAOUT6 | 25 | 26 | GND |
| DAOUT5 | 27 | 28 | GND |
| DAOUT4 | 29 | 30 | GND |
| DAOUT3 | 31 | 32 | GND |
| DAOUT2 | 33 | 34 | GND |
| DAOUT1 | 35 | 36 | GND |
| GND | 37 | 38 | GND |
| GND | 39 | 40 | GND |

J4 Power supply

Supply DC12V

| PIN | 1 | 2 | 3 |
|---|---|---|---|
| Use | 0V | OPEN | 12V |

JP1,JP3 RJ45 Connector for RiB serial line

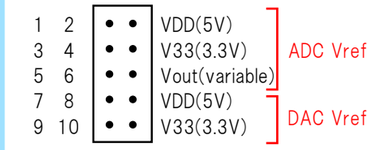
Although the connector is same with the ethernet (LAN), they have different electric characteristics, so DO NOT connect other ethernet devices to this connector.

| PIN | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 |
|---|---|---|---|---|---|---|---|---|
| Use | 12V | 12V | A | N/C | N/C | B | GND | GND |

JP4
RiB Serial termmination

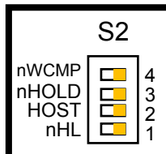
| JP4 | Terminal |
|---|---|
| Open | No |
| Short | Yes |

BR2 Reference voltage of ADC, DAC setting




**Active Low**

S2




Setting

(1) nHL

Communication method compatibility with HL10V/HL11V series.

When nHL is L, some of newly added methods for better reliability are disabled and RG20 can communicate with preceding RiB devices,

| nHL | HL10V/HL11compatibility |
|---|---|
| L | Compatible |
| H | Incompatible |

(4) nWCMP

Multi-cycle Data Verification

When nWCMP (double compare) is "L", RG20 compares data received from the serial line with the data of previous cycle, and RG20 accepts data only when both data matches.
This feature is designed for applications which require high data reliability or applications under noisy environments.

| nWCP | Multi-cycle Data Verification |
|---|---|
| L | ON |
| H | OFF |

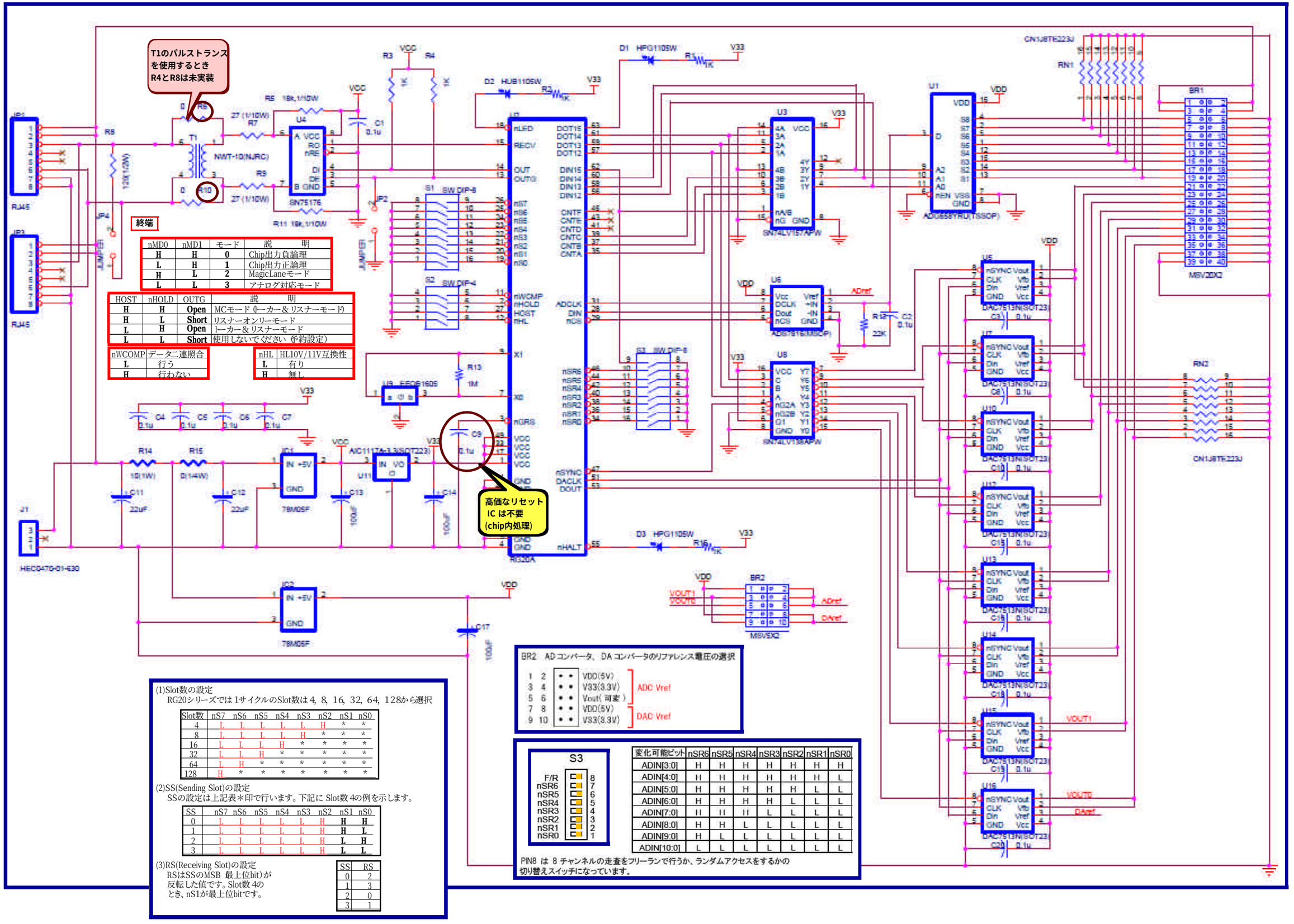
(2) HOST (HostMode Enable)
(3) nHOLD

JP3 OUTG Setting

| (4)HOST | (5)nHOLD | (JP3)OUTG | |
|---|---|---|---|
| H | H | Open | MC mode(Within talker and listener function) |
| | L | Short | Listener mode(High noise resistance setting) |
| L | H | Open | Talker & Listener mode |
| | L | Short | Out of use |

# RG20A_EVKIT 回路図

DD0-0800007A0




| nMD0 | nMD1 | モード | 説　明 |
|---|---|---|---|
| H | H | 0 | Chip出力負論理 |
| L | H | 1 | Chip出力正論理 |
| H | L | 2 | MagicLaneモード |
| L | L | 3 | アナログ対応モード |

| HOST | nHOLD | OUTG | 説　明 |
|---|---|---|---|
| H | H | Open | MCモード (トーカー & リスナーモード) |
| H | L | Short | リスナーオンリーモード |
| L | H | Open | トーカー & リスナーモード |
| L | L | Short | 使用しないでください（予約設定） |

| nWCOMP | データ二連照合 |
|---|---|
| L | 行う |
| H | 行わない |

| nHL | HL10V/11V互換性 |
|---|---|
| L | 有り |
| H | 無し |

(1)Slot数の設定
RG20シリーズでは 1サイクルのSlot数は 4, 8, 16, 32, 64, 128から選択

| Slot数 | nS7 | nS6 | nS5 | nS4 | nS3 | nS2 | nS1 | nS0 |
|---|---|---|---|---|---|---|---|---|
| 4 | L | L | L | L | L | H | * | * |
| 8 | L | L | L | L | H | * | * | * |
| 16 | L | L | L | H | * | * | * | * |
| 32 | L | L | H | * | * | * | * | * |
| 64 | L | H | * | * | * | * | * | * |
| 128 | H | * | * | * | * | * | * | * |

(2)SS(Sending Slot)の設定
SSの設定は上記表＊印で行います。下記に Slot数 4の例を示します。

| SS | nS7 | nS6 | nS5 | nS4 | nS3 | nS2 | nS1 | nS0 |
|---|---|---|---|---|---|---|---|---|
| 0 | L | L | L | L | L | H | **H** | **H** |
| 1 | L | L | L | L | L | H | **H** | **L** |
| 2 | L | L | L | L | L | H | **L** | **H** |
| 3 | L | L | L | L | L | H | **L** | **L** |

(3)RS(Receiving Slot)の設定
RSはSSのMSB（最上位bit)が反転した値です。Slot数 4のとき、nS1が最上位bitです。

| SS | RS |
|---|---|
| 0 | 2 |
| 1 | 3 |
| 2 | 0 |
| 3 | 1 |

BR2　ADコンバータ、DAコンバータのリファレンス電圧の選択

| | | | |
|---|---|---|---|
| 1 | 2 | VDD(5V) | ADC Vref |
| 3 | 4 | V33(3.3V) | |
| 5 | 6 | Vout(可変) | |
| 7 | 8 | VDD(5V) | DAC Vref |
| 9 | 10 | V33(3.3V) | |

S3

| | |
|---|---|
| F/R | 8 |
| nSR6 | 7 |
| nSR5 | 6 |
| nSR4 | 5 |
| nSR3 | 4 |
| nSR2 | 3 |
| nSR1 | 2 |
| nSR0 | 1 |

| 変化可能ビット | nSR6 | nSR5 | nSR4 | nSR3 | nSR2 | nSR1 | nSR0 |
|---|---|---|---|---|---|---|---|
| ADIN[3:0] | H | H | H | H | H | H | H |
| ADIN[4:0] | H | H | H | H | H | H | L |
| ADIN[5:0] | H | H | H | H | H | L | L |
| ADIN[6:0] | H | H | H | H | L | L | L |
| ADIN[7:0] | H | H | H | L | L | L | L |
| ADIN[8:0] | H | H | L | L | L | L | L |
| ADIN[9:0] | H | L | L | L | L | L | L |
| ADIN[10:0] | L | L | L | L | L | L | L |

PIN8 は 8 チャンネルの走査をフリーランで行うか、ランダムアクセスをするかの切り替えスイッチになっています。